Amendments to the Specification

The paragraph on page 1, beginning at line 6, has been amended as follows:

CROSS-REFERENCE TO RELATED APPLICATIONS

This patent application is a continuation of U.S. Patent Application Serial No. 10/325,525, filed December 19, 2002 now issued as U.S. Patent No. 6,697,975, which is a continuation of U.S. Patent Application Serial No. 09/430,456, filed October 29, 1999, now issued as U.S. Patent No. 6,546,520, which claims the benefit of the filing date of U.S. Provisional Patent Application Serial No. 60/106,482, filed October 30, 1998 and entitled EFFICIENT CONVOLUTIONAL INTERLEAVERS/DEINTERLEAVERS, the entire contents of which are hereby expressly incorporated by reference.

The paragraph at page 2, lines 14 to 22, is amended to read as follows:

The tension of this balance is most prominent in single-chip signal processing device implementations, where spatial efficiency can become a crucial consideration. There is a need for efficient implementations of certain types of interleavers/deinterleavers, including, for example, a Ramsey Type II device, which to date have not been demonstrated. Furthermore, there is a need for an interleaver/deinterleaver that can be dynamically reconfigurable among the different types of devices, for example, Ramsey I, Ramsey II, Ramsey III, and Ramsey IV.

The paragraph at page 6, lines 7 to 20, has been amended to read as follows:

Figure 1 illustrates an exemplary embodiment of a Ramsey Type II interleaver/deinterleaver. As shown in Figure 1, the present invention comprehends an interleaver 1, and a deinterleaver 2, that convey information through a data channel 3. Each of interleavers 1, 2 are shaped approximately like a triangular memory array. Interleaver 1 includes write commutator 4, read commutator 5, and plural rows 16, 17 of memory array 9. In general, each interleaver and deinterleaver have one write commutator and one read commutator. Interleaver 1 also includes row position pointer 11; it is desirable for each row 16, 17 in memory array 9 to have a row position pointer associated therewith. Deinterleaver 2 includes write commutator 6, read commutator 7, plural rows 18 of memory array 8, and row position pointer 13.

The paragraph at page 6, line 25 to page 7, line 7, is amended to read as follows:

In this example, commutators 4, 6 are write commutators, and commutators 5, 7 are read commutators. For the purposes of clarity, the following exemplary process will be

~~describe~~described from the perspective of interleaver 1; based on this information, a skilled practitioner can readily extend the process to deinterleaver 2. It is desirable, but not necessary, that commutators 4, 5 be initialized to the top row of the memory array. A symbol S_1 can be written at a first time to a first row 16 pointed to by write commutator 4. Also, symbol S_2 can be read at a second time, from second row 17 which is pointed to by read commutator 5. At this point, both pointers can be updated according to at least one predetermined update technique. It is desirable that read commutator 5 (and write commutator 6) be updated using a predetermined modulo technique. It is most desirable that a commutator "wraps" back on the array in an appropriate manner when the end of an array is reached.

The paragraph at page 7, lines 8 to 16, is amended to read as follows:

Commutator updates can be made using many schemes, one being:

$$\mathit{CommutatorPos}_{i+1} = (\mathit{CommutatorPos}_i + H) \bmod N$$

where: rows are labeled $0 \leq R < N$;

N is the total number of rows; and H can be either 1 or K, where K is computed by solving the equation:

$$KD \bmod N \equiv 1$$

where D is an interleave depth.

The paragraph at page 8, lines 6 to 17, is amended to read as follows:

The row position increment operation can include any method of successively pointing to individual memory locations in a given row 16, 17. One such method can include:

$$RowPos_{i+1} = \underline{(}RowPos_i + L\underline{)} \bmod RowSize$$

where **L** is an integer such that:

$$gcd(L, Rowsize) = 1$$

Other patterns and schemes may be used as well, for example, any such method which selects the elements in a given row, in any order. It is desirable that, once all elements have been selected, the selection sequence repeats.

The paragraph at page 10, lines 18 to 26, is amended to read as follows:

In the case where rows are sequentially indexed, it is apparent that the length of the rows so configured either remains the same or increases, as a result of the floor operation function. Similarly, the length of the rows in deinterleaver 2 will remain the same ~~of~~or increase. There is no requirement that the logical configuration of the memory correspond with the physical configuration, so that it is possible to substitute one row for another row. However, it is desirable that the interchanged rows be of the same length.